GENERAL DESCRIPTION

The Gigaram **GR2DF8B-E512XXX** is a 64M bit x 72 DDDR2 SDRAM high density Fully Buffered DIMM.
Fully Buffered DIMMs use commodity DRAMs isolated from the memory channel behind a buffer on the DIMM.
They are intended for use as main memory when installed in systems such as servers and workstations.
The Gigaram **GR2DF8B-E512XXX** consists of nine CMOS 64M x 8 DDR2 SDRAMs in 60/68-ball FBGA packages, mounted on a 240PIN glass-epoxy substrate.

DDR2 ECC REGISTERED DIMM PART INFORMATION

Part Number	Density	Speed	Organization	Component	Rank	Height
GR2DF8B-E512667	512MB	PC2-5300	64Mx72	64Mx8 * 9	1	30.35 mm
GR2DF8B-E512533	512MB	PC2-4200	64Mx72	64Mx8 * 9	1	30.35 mm

FEATURES

- Performance for DDR2-667 and DDR2-533

Part Number	DDR2-667	DDR2-533
Speed @ CL3	400MHz	400MHz
Speed @ CL4	533MHz	533MHz
Speed @ CL5	667MHz	533MHz
CL-tRCD-tRP	5-5-5	4-4-4

- 240-pin Fully Buffered ECC Dual-In-Line DDR2 SDRAM Module
- Module Organization: one rank, 64Mx72
- JEDEC standard DDR2 SDRAMs with 1.8V ± 0.1V Power Supply
- Re-drive and re-sync of all address, command, clock and data signals using AMB (Advanced Memory Buffer)
- High speed Differential Point-to-Point Link Interface at 1.5V.
- Host Interface and AMB component industry standard compliant.
- Supports SMBus protocol interface for access to the AMB configuration registers.
- Detects errors on the channel and reports them to the host memory controller.
- Automatic DDR2 DRAM Bus Calibration.
- Full Host Control of DDR2 DRAMs.
- Over-Temperature Detection and Alert.
- Hot Add-on and Hot Remove Capability.
- MBIST and IBIST Test Functions.
- Transparent mode for DRAM test support.
- Low profile: 133.35mm x 30.35mm
- RoHS Compliant Product

ADDRESS CONFIGURATION

Organization	Row Address	Column Address	Bank Address	Auto Precharge
64Mx8 (512Mb) based module	A0-A13	A0-A9	BA0-BA1	A10

PIN CONFIGURATIONS (Front Side/ Back Side)

Pin	FRONT	Pin	BACK	Pin	FRONT	Pin	BACK
1	VDD	121	VDD	62	VSS	182	VSS
2	VDD	122	VDD	63	PN10	183	SN10
3	VDD	123	VDD	64	/PN10	184	/SN10
4	VSS	124	VSS	65	VSS	185	VSS
5	VDD	125	VDD	66	PN11	186	SN11
6	VDD	126	VDD	67	/PN11	187	/SN11
7	VDD	127	VDD	68	VSS	188	VSS
8	VSS	128	VSS	KEY		KEY	
9	VCC	129	VCC	69	VSS	189	VSS
10	VCC	130	VCC	70	PS0	190	SS0
11	VSS	131	VSS	71	/PS0	191	/SS0
12	VCC	132	VCC	72	VSS	192	VSS
13	VCC	133	VCC	73	PS1	193	SS1
14	VSS	134	VSS	74	/PS1	194	/SS1
15	VTT	135	VTT	75	VSS	195	VSS
16	VID1	136	VID0	76	PS2	196	SS2
17	/RESET	137	DNU/M_TEST	77	/PS2	197	/SS2
18	VSS	138	VSS	78	VSS	198	VSS
19	RFU**	139	RFU**	79	PS3	199	SS3
20	RFU**	140	RFU**	80	/PS3	200	/SS3
21	VSS	141	VSS	81	VSS	201	VSS
22	PN0	142	SN0	82	PS4	202	SS4
23	/PN0	143	/SN0	83	/PS4	203	/SS4
24	VSS	144	VSS	84	VSS	204	VSS
25	PN1	145	SN1	85	VSS	205	VSS
26	/PN1	146	/SN1	86	RFU*	206	RFU*
27	VSS	147	VSS	87	RFU*	207	RFU*
28	PN2	148	SN2	88	VSS	208	VSS
29	/PN2	149	/SN2	89	VSS	209	VSS
30	VSS	150	VSS	90	PS9	210	SS9
31	PN3	151	SN3	91	/PS9	211	/SS9
32	/PN3	152	/SN3	92	VSS	212	VSS
33	VSS	153	VSS	93	PS5	213	SS5
34	PN4	154	SN4	94	/PS5	214	/SS5
35	/PN4	155	/SN4	95	VSS	215	VSS
36	VSS	156	VSS	96	PS6	216	SS6
37	PN5	157	SN5	97	/PS6	217	/SS6
38	/PN5	158	/SN5	98	VSS	218	VSS
39	VSS	159	VSS	99	PS7	219	SS7
40	PN13	160	SN13	100	/PS7	220	/SS7
41	/PN13	161	/SN13	101	VSS	221	VSS
42	VSS	162	VSS	102	PS8	222	SS8
43	VSS	163	VSS	103	/PS8	223	/SS8
44	RFU*	164	RFU*	104	VSS	224	VSS
45	RFU*	165	RFU*	105	RFU**	225	RFU**
46	VSS	166	VSS	106	RFU**	226	RFU**
47	VSS	167	VSS	107	VSS	227	VSS
48	PN12	168	SN12	108	VDD	228	SCK
49	/PN12	169	/SN12	109	VDD	229	/SCK
50	VSS	170	VSS	110	VSS	230	VSS
51	PN6	171	SN6	111	VDD	231	VDD
52	/PN6	172	/SN6	112	VDD	232	VDD
53	VSS	173	VSS	113	VDD	233	VDD
54	PN7	174	SN7	114	VSS	234	VSS
55	/PN7	175	/SN7	115	VDD	235	VDD
56	VSS	176	VSS	116	VDD	236	VDD
57	PN8	177	SN8	117	VTT	237	VTT
58	/PN8	178	/SN8	118	SA2	238	VDDSPD
59	VSS	179	VSS	119	SDA	239	SA0
60	PN9	180	SN9	120	SCL	240	SA1
61	/PN9	181	/SN9				

***** These pin positions are reserved for forwarded clocks to be used in future module implementations

** These pin positions are reserved for future architecture flexibility

FB DIMM INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Polarity	Function
Channel Signals			
SCK, /SCK	Input	Differential	System Clock Input
PN[13:0], /PN [13:0]	Output	Differential	Primary Northbound Data
PS[9:0], /PS[9:0]	Input	Differential	Primary Southbound Data
SN[13:0], /SN [13:0]	Input	Differential	Secondary Northbound Data
SS[9:0], /SS[9:0]	Output	Differential	Secondary Southbound Data
SMB Bus Signals			
SA [2:0]	Input	-	SPD Address, also used to select the DIMM number in the AMB
SDA	I/O	-	SPD Data, A resistor must be connected from the SDA bus line to VDDSPD on the system planar to act as a pull-up
SCL	Input	-	SPD Clock
Miscellaneous Signals			
/RESET	Input	Active Low	AMB Reset Signal
VID[1:0]	Input	-	Voltage ID. Both pins shall be NC in case of VDD=1.8V, Vcc=1.5V
TEST	Analog	+0.9V	DRAM Vref Margin Test. Do not connect on the system planar.
Power / Ground			
VDD	Supply	+1.8V	DDR2 Dram power
VCC	Supply	+1.5V	AMB Core power
V_{DDSPD}	Supply	+3.3V	SPD power

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limit Values		Unit	Note
		Min.	Max.		
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	-0.3	1.75	V	1
Voltage on V_{CC} relative to V_{SS}	V_{CC}	-0.3	1.75	V	1
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-0.5	2.3	V	1
Voltage on V_{TT} relative to V_{SS}	V_{TT}	-0.5	2.3	V	1
Storage temperature range	T_{STG}	-55	+100	° C	1
DDR2 SDRAM device operating temperature (Ambient)	T_{CASE}	0	85	° C	1, 2
		85	95		
AMB device operating temperature (Ambient)	T_j	0	110	° C	1, 2

Note:1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. DDR2 SDRAMs of FBDIMM should require this specification.

Parameter	Symbol		DRAM	Units
Average periodic refresh interval	tREFI	$0\,°C \le T_{CASE} \le 85°C$	7.8	µs
		$85\,°C < T_{CASE} \le 95°C$	3.9	µs

OPERATING TEMPERATURE RANGE

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
DRAM Component Case Temperature Range	T_{CASE}	0	+95	° C	1, 2, 3, 4
AMB Component Case Temperature Range	T_{CASE}	0	+110	° C	1

Note: 1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Within the DRAM Component Case Temperature range all DRAM specification will be supported.
3. Above 85 ° C DRAM case temperature the Auto-Refresh command interval has to be reduced to tREF1= 3.9us.
4. Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85 ° C case temperature before initiating self-refresh operation.

INPUT DC OPERATING CONDITIONS

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Norm.	Max.		
AMB supply Voltage	V_{CC}	1.455	1.50	1.575	V	
DDR2 SDRAM Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Termination Voltage	V_{TT}	0.48 x V_{DD}	0.50 x V_{DD}	0.52 x V_{DD}	V	
EEPROM supply Voltage	V_{DDSPD}	3.0	3.3	3.6	V	
SPD Input HIGH (logic1) Voltage	$V_{IH(DC)}$	-	-	V_{DDSPD}	V	1
SPD Input LOW (logic0) Voltage	$V_{IL(DC)}$	1.0	-	0.8	V	1
RESET Input HIGH (logic1) Voltage	$V_{IH(DC)}$	-	-	-	V	2
RESET Input LOW (logic0) Voltage	$V_{IL(DC)}$	-	-	0.5	V	1
Leakage Current (RESET)	I_L	-90	-	90	uA	2
Leakage Current (link)	I_L	-5	-	5	uA	3

Note: 1. Applies for SMB and SPD bus signals.
2. Applies for AMB CMOS signal RESET#.
3. For other AMB related DC parameters, please refer to the high-speed differential link interface specification.

TIMING PARAMETERS

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Norm.	Max.		
EI Assertion Pass-Thru Timing	$t_{EI\ Propagatet}$			4	clks	-
EI Deassertion Pass-Thru Timing	t_{EID}			Bitlock	Clks	2
EI Assertion Duration	t_{EI}	100			Clks	1, 2
FBD Cmd to DDR Clk out that latches Cmd			8.1		ns	3
FBD Cmd t DDR Write			TBD		ns	
DDR Read to FBD (last DIMM)			5.0		ns	4
Resample Pass-Thru time			1.075		ns	
ResynchPass-Thru time			2.075		ns	
Bit Lock Interval	$t_{BitLock}$			119	frames	1
Frame Lock Interval	$t_{FrameLock}$			154	frames	1

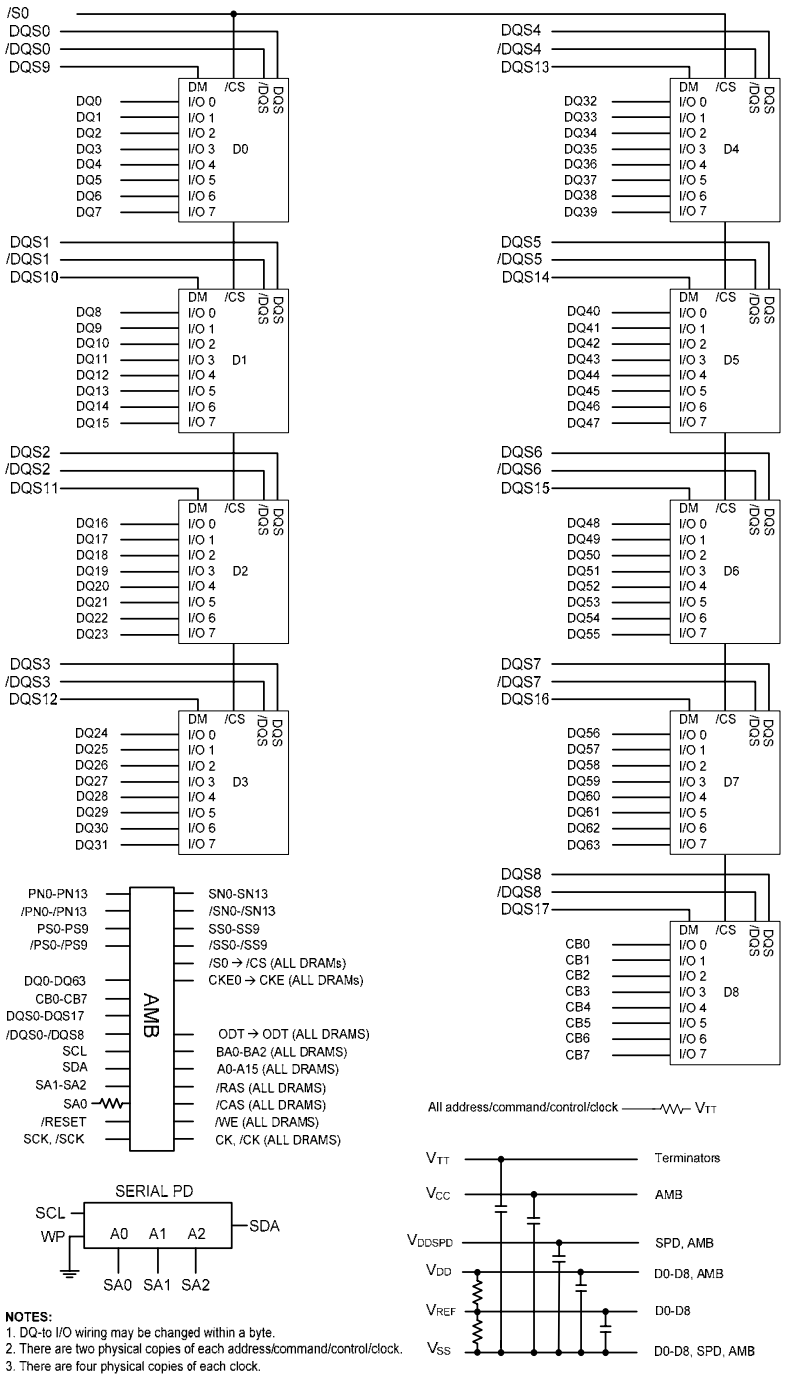
Note: 1. Defined in FB-DIMM Architecture and Protocol Spec.
2. Clocks defined as core clocks=2x SCK input
3. @DDR2-667 – measured from beginning of frame at southbound input to DDR clock output that latches the first command of a frame to the DRAMs.
4. @DDR2-667 – measured from latest DQS input AMB to start of matching data frame at northbound FB-DIMM outputs.

I_{CC} / I_{DD} SPECIFICATION FOR FB-DIMM

Symbol	PC2-4200	PC2-5300	Unit	Note
I_{CC}_Idle_0	1,890	2,210	mA	
P_{CC}_Idle_0	2.8	3.27	W	
I_{DD}_Idle_0	690	720	mA	
P_{DD}_Idle_0	1.22	1.29	W	
I_{TOT}_Idle_0	2,580	2,930	mA	
P_{TOT}_Idle_0	4.03	4.55	W	
I_{CC}_Idle_1	2,420	2,820	mA	
P_{CC}_Idle_1	3.55	4.12	W	
I_{DD}_Idle_1	690	730	mA	
P_{DD}_Idle_1	1.23	1.3	W	
I_{TOT}_Idle_1	3,100	3,540	mA	
P_{TOT}_Idle_1	4.78	5.41	W	
I_{CC}_Active_1	2,610	3,010	mA	
P_{CC}_Active_1	3.83	4.4	W	
I_{DD}_Active_1	2,100	2,030	mA	
P_{DD}_Active_1	3.74	3.62	W	
I_{TOT}_Active_1	4,710	5,040	mA	
P_{TOT}_Active_1	7.56	8.01	W	
I_{CC}_Active_2	0	0	mA	
P_{CC}_Active_2	0	0	W	
I_{DD}_Active_2	0	0	mA	
P_{DD}_Active_2	0	0	W	
I_{TOT}_Active_2	0	0	mA	
P_{TOT}_Active_2	0	0	W	
I_{CC_IBIST}	3,250	3,820	mA	
P_{CC_IBIST}	4.76	5.56	W	
I_{DD_IBIST}	650	690	mA	
P_{DD_IBIST}	1.16	1.23	W	
I_{TOT_IBIST}	3,900	4,500	mA	
P_{TOT_IBIST}	5.91	6.78	W	
$I_{CC\_Training}$	2,960	3,470	mA	
$P_{CC\_Training}$	4.35	5.06	W	
$I_{DD\_Training}$	650	690	mA	
$P_{DD\_Training}$	1.16	1.23	W	
$I_{TOT\_Training}$	3,610	4,150	mA	
$P_{TOT\_Training}$	5.5	6.28	W	
I_{CC_EI}	1,310	1,570	mA	
P_{CC_EI}	1.94	2.32	W	
I_{DD_EI}	120	120	mA	
P_{DD_EI}	0.2	0.21	W	
I_{TOT_EI}	1,420	1,690	mA	
P_{TOT_EI}	2.14	2.53	W	
$I_{CC\_MEMBIST}$	2,620	3,030	mA	
$P_{CC\_MEMBIST}$	3.84	4.43	W	
$I_{DD\_MEMBIST}$	2,260	2,320	mA	
$P_{DD\_MEMBIST}$	4.03	4.12	W	
$I_{TOT\_MEMBIST}$	4,880	5,340	mA	
$P_{TOT\_MEMBIST}$	7.87	8.54	W	

Note: The power is calculated as follows: Pcc=Vcc x Icc where Vcc=1.5V

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. DQ-to I/O wiring may be changed within a byte.
2. There are two physical copies of each address/command/control/clock.
3. There are four physical copies of each clock.

PACKAGE DIMENSION (WITH FULL HEAT SINK)