DDR ECC REGISTERED DIMM

512MB: 64Mx72 based on 32Mx8 DDR SDRAM

GR75020-E512/400 (PC3200)
GR75020-E512/333 (PC2700)
GR75020-E512/266 (PC2100)

Registered 184pin DIMM
72-bit ECC

GR75020-E512/xxx

GR75020-E512/xxx ECC Registered DDR SDRAM 184pin DIMM
64Mx72 DDR SDRAM based on 32Mx8

GENERAL DESCRIPTION

The Gigaram GR75020-E512 is 64M bit x 72 Double Data Rate SDRAM high density memory modules. The Gigaram GR75020-E512 consists of eighteen CMOS 32M x 8bit with 4banks Double Data Rate SDRAMs in 66pin TSOP-II (400mil) packages, mounted on a 184pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM. The GR75020-E512 is Dual In-Line Memory Modules and intended for mounting into 184pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory systems applications.

FEATURE

* SPEED

PC2100	133MHz/266Mbps @CL2.0, CL2.5
PC2700	166MHz/333Mbps @CL2.5
PC3200	200MHz/400Mbps @CL3.0

* Power supply: Vdd : 2.5V ± 0.2V, Vddq : 2.5V ± 0.2 V
* Double-data-rate architecture; two data transfers per clock cycle
* Bi-directional data strobe (DQS)
* Differential clock inputs (CK and /CK)
* DLL aligns DQ and DQS transition with CK transition
* Programmable read latency 2.0, 2.5, 3.0 (clock)
* Programmable burst length (2, 4, 8)
* Programmable burst type (sequential & interleave)
* Edge aligned data output, center aligned data input
* Auto & self-refresh, 7.8us refresh interval (8K/64ms refresh)
* Serial Presence Detect with EEPROM
* PCB: **Height 1150mil**, double sided component.

PIN CONFIGURATIONS (Front Side/ Back Side)

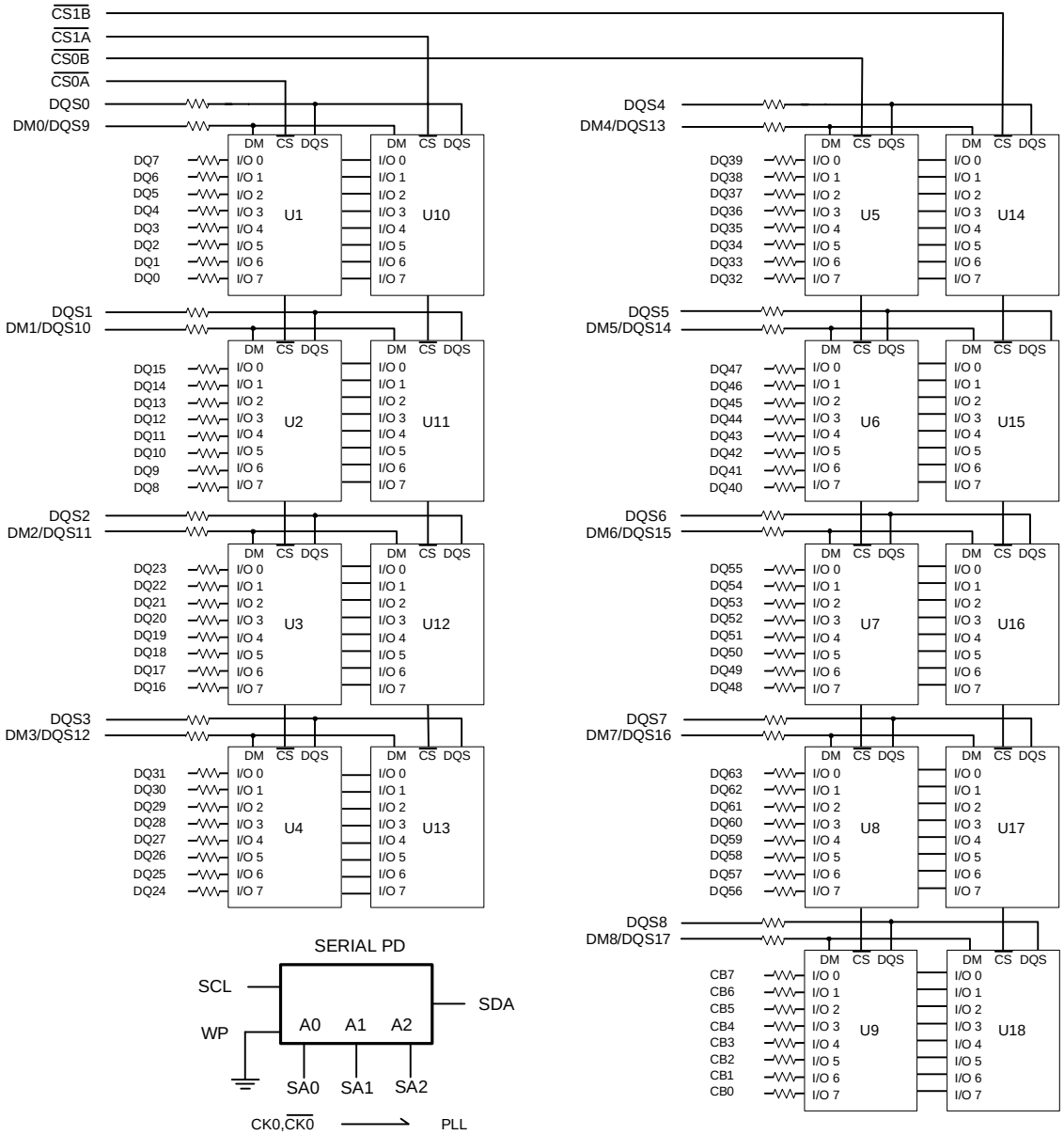
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	/RAS
2	DQ0	33	DQ24	63	/WE	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	/CAS	96	VDDQ	127	DQ29	157	/CS0
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	/CS1
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	/RESET	41	A2	71	*1/CS2	102	NC	133	DQ31	163	*1/CS3
11	VSS	42	VSS	72	DQ48	103	*1A13	134	CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5	165	DQ52
13	DQ9	44	CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1	75	*1CK2	106	DQ13	137	CK0	167	NC
15	VDDQ	46	VDD	76	*1/CK2	107	DM1	138	/CK0	168	VDD
16	*1CK1	47	DQS8	77	VDDQ	108	VDD	139	VSS	169	DM6
17	*1/CK1	48	A0	78	DQS6	109	DQ14	140	DM8	170	DQ54
18	VSS	49	CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	CB6	172	VDDQ
20	DQ11	51	CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	*1BA2	144	CB7	174	DQ60
22	VDDQ	KEY		83	DQ56	114	DQ20	KEY		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

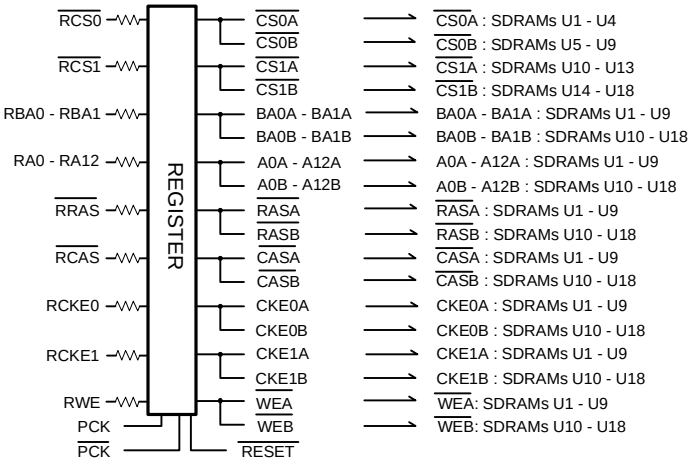
* These pins are not used in this module.

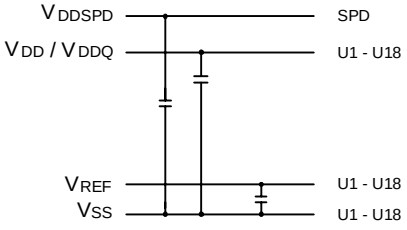
PIN DESCRIPTION

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Bank Selected Address
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit(Data-in/Data-out)
DQS0 ~ DQS8	Data Strobe input/output
CK0, /CK0	Clock input
CKE0, CKE1	Clock enable input
/CS0, /CS1	Chip select input
/RAS	Row address strobe
/CAS	Column address strobe
/WE	Write enable
DM0 ~ DM8	Data -in Mask
VDD	Power supply (2.5V)
VDDQ	Power supply for DQS (2.5V)
VSS	Ground
VREF	Power supply for reference
VDDSPD	Serial EEPROM Power supply (2.3V to 3.6V)
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
VDDID	VDD identification flag
/RESET	Reset enable
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



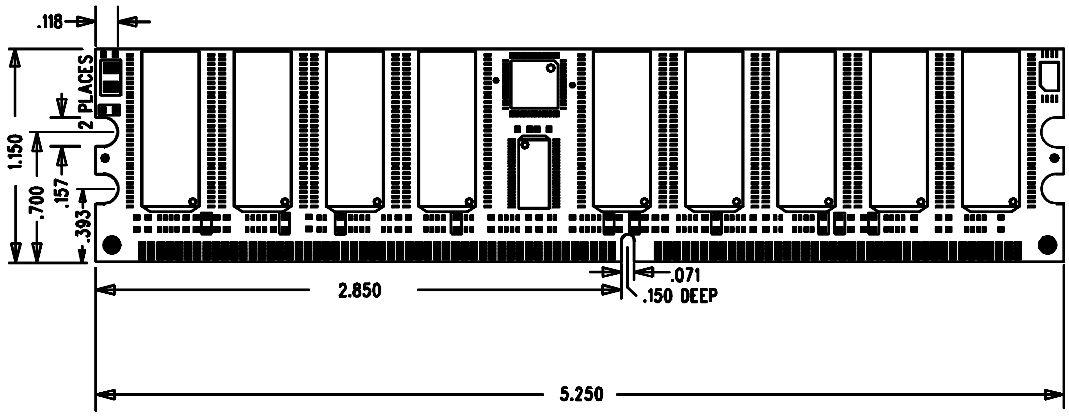




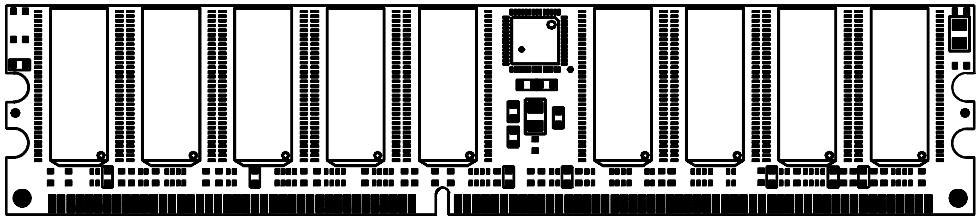
NOTES:
1. DQ to I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS Registers: 22 Ohms.

PACKAGE DIMENSIONS

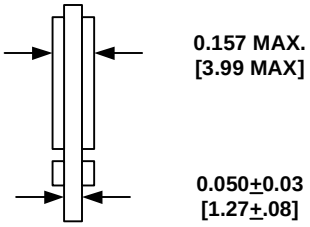
FRONT VIEW



BACK VIEW



SIDE VIEW



- Tolerances: ±0.005 (.13 mm) unless otherwise specified.
- The used device is 32Mx8 DDR SDRAM TSOP II